VT1802

120-CHANNEL SINGLE-ENDED, 60-CHANNEL DIFFERENTIAL +28 V / 73 V I/O CURRENT DRIVER

USER'S MANUAL

P/N: 82-0106-000
Rev. February 13, 2007

VXI Technology, Inc.

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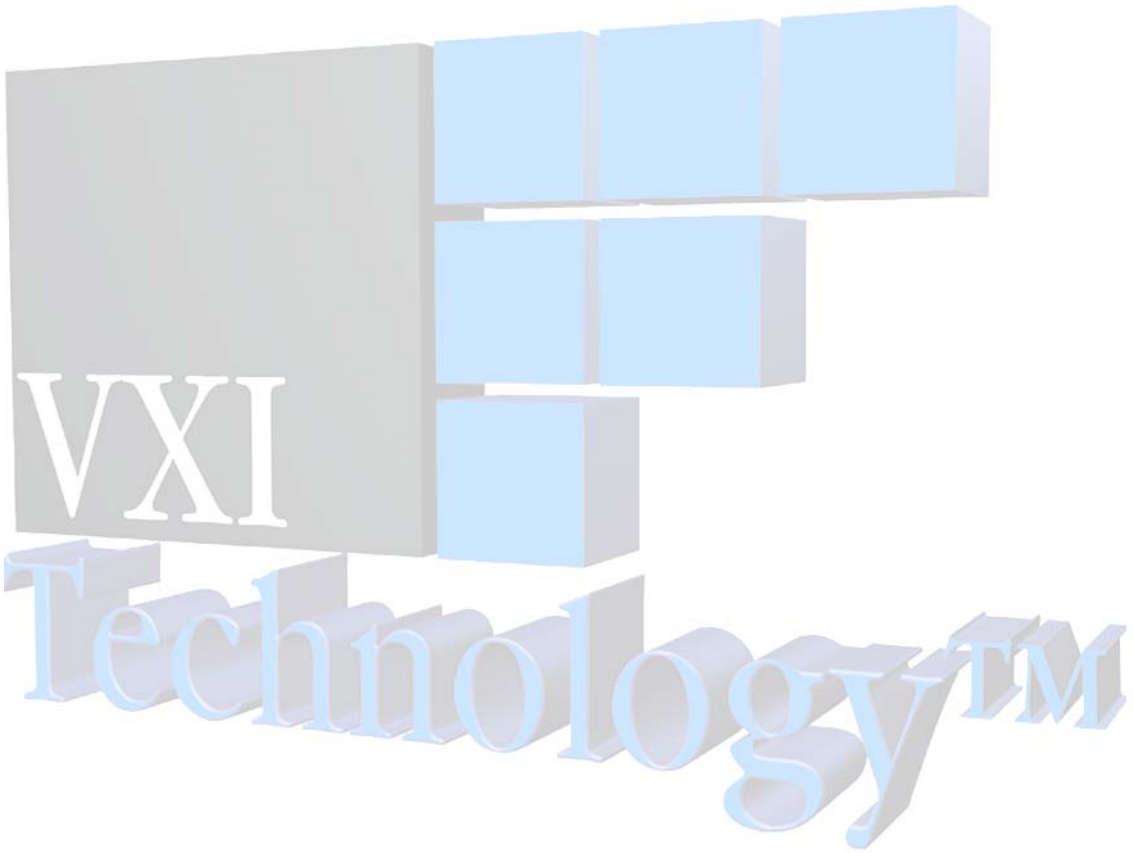
VXI
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CERTIFICATION

VXI Technology, Inc. (VTI) certifies that this product met its published specifications at the time of shipment from the factory. VTI further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility and to the calibration facilities of other International Standards Organization members.

WARRANTY

The product referred to herein is warranted against defects in material and workmanship for a period of three years from the receipt date of the product at customer's facility. The sole and exclusive remedy for breach of any warranty concerning these goods shall be repair or replacement of defective parts, or a refund of the purchase price, to be determined at the option of VTI.

For warranty service or repair, this product must be returned to a VXI Technology authorized service center. The product shall be shipped prepaid to VTI and VTI shall prepay all returns of the product to the buyer. However, the buyer shall pay all shipping charges, duties, and taxes for products returned to VTI from another country.

VTI warrants that its software and firmware designated by VTI for use with a product will execute its programming when properly installed on that product. VTI does not however warrant that the operation of the product, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The warranty shall not apply to defects resulting from improper or inadequate maintenance by the buyer, buyer-supplied products or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

VXI Technology, Inc. shall not be liable for injury to property other than the goods themselves. Other than the limited warranty stated above, VXI Technology, Inc. makes no other warranties, express or implied, with respect to the quality of product beyond the description of the goods on the face of the contract. VTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

RESTRICTED RIGHTS LEGEND

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subdivision (b)(3)(ii) of the Rights in Technical Data and Computer Software clause in DFARS 252.227-7013.

VXI Technology, Inc.
2031 Main Street
Irvine, CA 92614-6509 U.S.A.

DECLARATION OF CONFORMITY

Declaration of Conformity According to ISO/IEC Guide 22 and EN 45014

MANUFACTURER'S NAME	VXI Technology, Inc.
MANUFACTURER'S ADDRESS	2031 Main Street Irvine, California 92614-6509
PRODUCT NAME	120 single-ended, 60 differential channel current driver
MODEL NUMBER(S)	VT1802
PRODUCT OPTIONS	All
PRODUCT CONFIGURATIONS	All

VXI Technology, Inc. declares that the aforementioned products conform to the requirements of the Low Voltage Directive 73/23/EEC *and the* EMC Directive 89/366/EEC *(inclusive* 93/68/EEC*) and carries the "CE" mark accordingly. The products have been designed and manufactured according to the following specifications:*

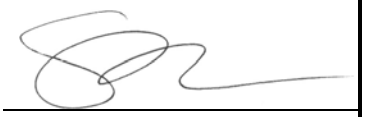
SAFETY	EN61010 (2001)
EMC	EN61326 (1997 w/A1:98) Class A CISPR 22 (1997) Class A VCCI (April 2000) Class A ICES-003 Class A (ANSI C63.4 1992) AS/NZS 3548 (w/A1 & A2:97) Class A FCC Part 15 Subpart B Class A EN 61010-1:2001

The products were installed into a C-size VXI mainframe chassis and tested in a typical configuration.

I hereby declare that the aforementioned products have been designed to comply with the relevant sections of the specifications listed above as well as complying with all essential requirements of the Low Voltage Directive.

February 2007

CE



Steve Mauga, QA Manager

GENERAL SAFETY INSTRUCTIONS

Review the following safety precautions to avoid bodily injury and/or damage to the product. These precautions must be observed during all phases of operation or service of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the product.

Service should only be performed by qualified personnel.

TERMS AND SYMBOLS

These terms may appear in this manual:

WARNING Indicates that a procedure or condition may cause bodily injury or death.

CAUTION Indicates that a procedure or condition could possibly cause damage to equipment or loss of data.

These symbols may appear on the product:

ATTENTION - Important safety instructions

Frame or chassis ground

Indicates that the product was manufactured after August 13, 2005. This mark is placed in accordance with *EN 50419, Marking of electrical and electronic equipment in accordance with Article 11(2) of Directive 2002/96/EC (WEEE).* End-of-life product can be returned to VTI by obtaining an RMA number. Fees for take-back and recycling will apply if not prohibited by national law.

WARNINGS

Follow these precautions to avoid injury or damage to the product:

Use Proper Power Cord To avoid hazard, only use the power cord specified for this product.

Use Proper Power Source To avoid electrical overload, electric shock or fire hazard, do not use a power source that applies other than the specified voltage.

Use Proper Fuse To avoid fire hazard, only use the type and rating fuse specified for this product.

WARNINGS (CONT.)

Avoid Electric Shock

To avoid electric shock or fire hazard, do not operate this product with the covers removed. Do not connect or disconnect any cable, probes, test leads, etc. while they are connected to a voltage source. Remove all power and unplug unit before performing any service. ***Service should only be performed by qualified personnel.***

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground.

Operating Conditions

To avoid injury, electric shock or fire hazard:

- Do not operate in wet or damp conditions.
- Do not operate in an explosive atmosphere.
- Operate or store only in specified temperature range.
- Provide proper clearance for product ventilation to prevent overheating.
- DO NOT operate if any damage to this product is suspected. ***Product should be inspected or serviced only by qualified personnel.***

Improper Use

The operator of this instrument is advised that if the equipment is used in a manner not specified in this manual, the protection provided by the equipment may be impaired.
Conformity is checked by inspection.

SUPPORT RESOURCES

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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SECTION 1

INTRODUCTION

OVERVIEW

The VT1802 is a high-performance high voltage I/O module with ten groups of 12 channels for a total of 120 channels per module. Each group of channels may be configured as an input or output under program control. Individual channels can be set to tri-state mode. In the output mode, each group can be configured with either 28 V or 73 V levels. Logic programmability (high/low) is on a per channel basis. Two level sensitive trigger inputs provide the flexibility to set external input conditions that must be met before a channel is enabled.

The VT1802 is an ideal module for multiple channel I/O applications which require the capability to source up to 140 mA per channel. Each channel has built-in over-current protection ensuring that the board will not be damaged if its specifications are exceeded.

VT1802 SPECIFICATIONS

REQUIREMENTS	
CHANNELS	
	120 single-ended, 60 differential
VOLTAGE LEVELS	
28 V (dc)	0 V or +28 V (±1.0 V)
73 V (dc)	2.5 V or +73 V (±1.0 V)
CURRENT[1]	
28 V (dc)	140 mA maximum
73 V (dc)	1.0 mA maximum
MAXIMUM LOAD[2]	
@ 28 V (dc), 140 mA	84 channels, and
@ 73 V (dc), 1 mA	24 channels
RISE/FALL TIME	
28 V (dc)	<1 ms
73 V (dc)	<2 ms
TRIGGER INPUTS	
External Triggers[3,4,5]	Two simultaneous TTL
High State	2.4 V minimum. Cannot exceed 5 V.
Low State	0.4 V maximum. Must be greater than 0 V.
Internal Triggers	Eight VXI backplane TTL triggers
Software Triggers	Via the soft front panel
LOGIC PROGRAMMABILITY	
	individual channel
AMPLITUDE PROGRAMMABILITY	
	12 channels/group
CONNECTOR TYPES	
Current Driver	160-pin connector
Power	2-pin D-sub connector
COOLING	
Worst Case	150 W
TRI-STATE	
	Per channel
OVER-CURRENT PROTECTION	
	Per channel

NOTE

1) External power supply required.
2) Assumes worst case air flow (i.e. 6-slot chassis with all slots open). The temperature rise is 6 °C less in a 13-slot chassis. Temperature rise can be lowered significantly if unused slots are covered.
3) If the external trigger experiences a voltage between 0.4 V and 2.4 V, the VT1802 may enter an indeterminate state. Measures should be taken to ensure that these conditions do not occur.
4) The external triggers are active-high level triggers that should be driven by a 5 V TTL signal. The signal must be free of glitches and stay in the high or low state for a minimum of 200 ns.
5) If the VT1802 external trigger experiences a voltage of greater than 6 V, damage will occur to the VT1802.

SECTION 2

PREPARATION FOR USE

INTRODUCTION

When the VT1802 is unpacked from its shipping carton, the contents should include the following items:

(1) VT1802 module
(1) VT1802 User's Manual (this manual)

All components should be immediately inspected for damage upon receipt of the unit.

The chassis should be checked to ensure that it is capable of providing adequate power and cooling for the VT1802. Once the chassis is found adequate, the VT1802's logical addresses and the backplane jumpers of the chassis should be configured prior to the VT1802's installation. After the VT1802 is assessed to be in good condition, it may be installed into an appropriate C-size or D-size VXIbus chassis in any slot other than slot zero.

CALCULATING SYSTEM POWER AND COOLING REQUIREMENTS

It is imperative that the chassis provide adequate power and cooling for this module. Referring to the chassis operation manual, confirm that the power budget for the system (the chassis and all modules installed therein) is not exceeded and that the cooling system can provide adequate airflow at the specified backpressure.

It should be noted that if the chassis cannot provide adequate power to the module, the instrument might not perform to specification or possibly not operate at all. In addition, if adequate cooling is not provided, the reliability of the instrument will be jeopardized and permanent damage may occur. Damage found to have occurred due to inadequate cooling could also void the warranty of the module.

SETTING THE CHASSIS BACKPLANE JUMPERS

Please refer to the chassis operation manual for further details on setting the backplane jumpers.

SWITCH SETTINGS

The VT1802 has three configurable switches, all located at the top of the unit near the rear connectors. The two rotary dials (S1 and S2) located closest to the rear of the interface card set the logical address (LA) for the module, while the two-position DIP switch (S3) sets the extended memory space for the module to either A24 or A32. Figure 1-1 below shows the location of these switches and the following paragraphs explain how they are configured.

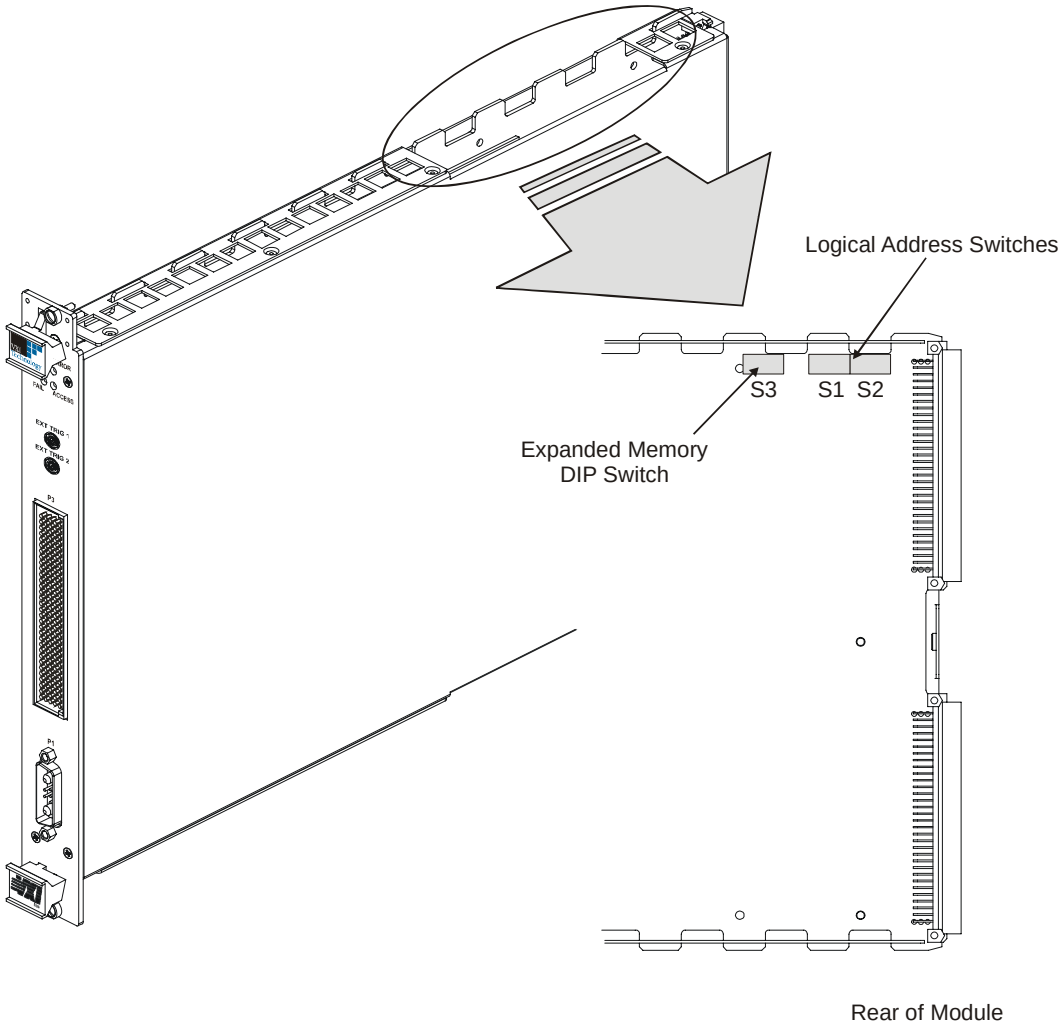

FIGURE 1-1: SWITCH LOCATIONS

Setting the Logical Address

The LA of the VT1802 is set by two rotary switches with each switch labeled with positions 0 through F. *S1*, the switch closer to the front panel of the module, is the least significant bit (**LS** or "**Front**"), and *S2*, the switch located towards the back of the module, is the most significant bit (**MS** or "**Back**"). To set the LA, simply rotate the pointer to the desired value. For example, to set the LA to **25**, first convert the decimal number to the hexadecimal value of **19**. Next, set the back switch to **1** and the front switch to **9**. See Figure 1-2. Here are a couple of conversion examples:

Example 1

LA (decimal)	Divide by 16		MS	LS	
25	25 / 16	=	1	w/ 9 remaining	*Divide the decimal value by 16 to get the MS and the LS.*
		=	0001	1001	*The 1 is the MS, and the remainder of 9 is the LS.*
		=	1	9	*Convert to hexadecimal. Set the back switch to 1 and the front switch to 9.*

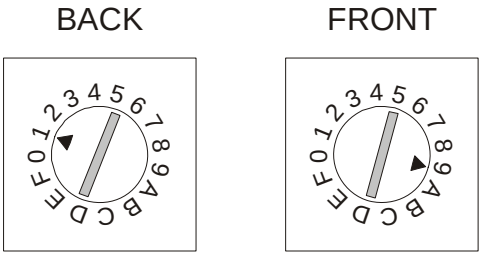

FIGURE 1-2: LOGICAL ADDRESS EXAMPLE 1

Here is another way of looking at the conversion:

LA = (back switch x 16) + front switch
LA = (1 x 16) + 9
LA = 16 + 9
LA = 25

Example 2

LA (decimal)	Divide by 16		MS	LS	
200	200 / 16	=	12	w/ 8 remaining	*Divide by 16.*
		=	1100	1000	*Convert to MS and LS.*
		=	C	8	*Convert to hexadecimal. Set the back switch to C and the front switch to 8.*

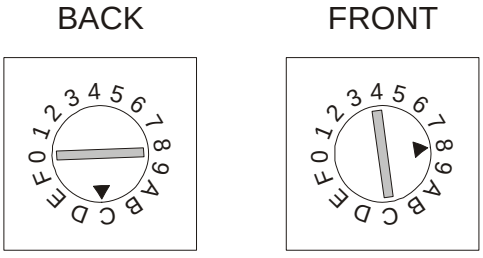

FIGURE 1-3: LOGICAL ADDRESS EXAMPLE 2

Set the address switches to **FF** (factory default) for dynamic configuration. Upon power-up, the resource manager will assign a logical address. See "Section F - Dynamic Configuration" in the *VXIbus Specification* for further information.

There is only one logical address per VT1802 base unit. Address assignments for individual modules are handled through the A24/A32 address space allocation (see *Description of VT1802 Module Registers - A24 / A32 - Extended Memory* for more information).

Selecting the Extended Memory Space

The *extended memory space* of VT1802 base units is set by a DIP switch that is located on the top edge of the interface card (see Figure 1-1). Position 1, located to the left on the DIP switch, selects between A24 and A32 memory address space. In the UP position, the VT1802 will request A24 space. In the DOWN position (factory default), the VT1802 will request A32 space. (Position 2 is not currently used.) The selection of the address space should be based upon the memory allocation requirements of the system that the VT1802 module will be installed. The amount of memory allocated to a VT1802 module is independent of the address space selected.

NOTE	GPIB slot 0 controllers will not support the VT1802 as configured from the factory as they do not support dynamically configured logical addresses or A32 address space. The VT1802 can be reconfigured to support GPIB slot 0s by setting the logical address switches to a static address and having the address space configured for A24. If using a slot 0 controller that supports A32 extended memory space, it is recommended that the switches be left in their factory configured state to take advantage of the greater available address space capacity.

SECTION 3

MODULE USE AND OPERATION

OVERVIEW

The VT1802 is a current driver module, providing 10 banks of 12 channels (120 channels) from two constant voltage sources. Each bank of twelve channels may be configured as a current source or a current sink of different voltages under software program control. The channels can be used in either single-ended of differential mode.

The VT1802 contains two identical sections with five banks (60 channels) a piece. The control functions divided into three sections:

Backplane Interface

Output Control	Enable Channel Output Select Channel Level Select Bank Voltage Over-current Status
Output Monitor	Output Threshold Voltage Channel Output Level Status (Readback)

See Figure 2-1 illustrates these divisions.

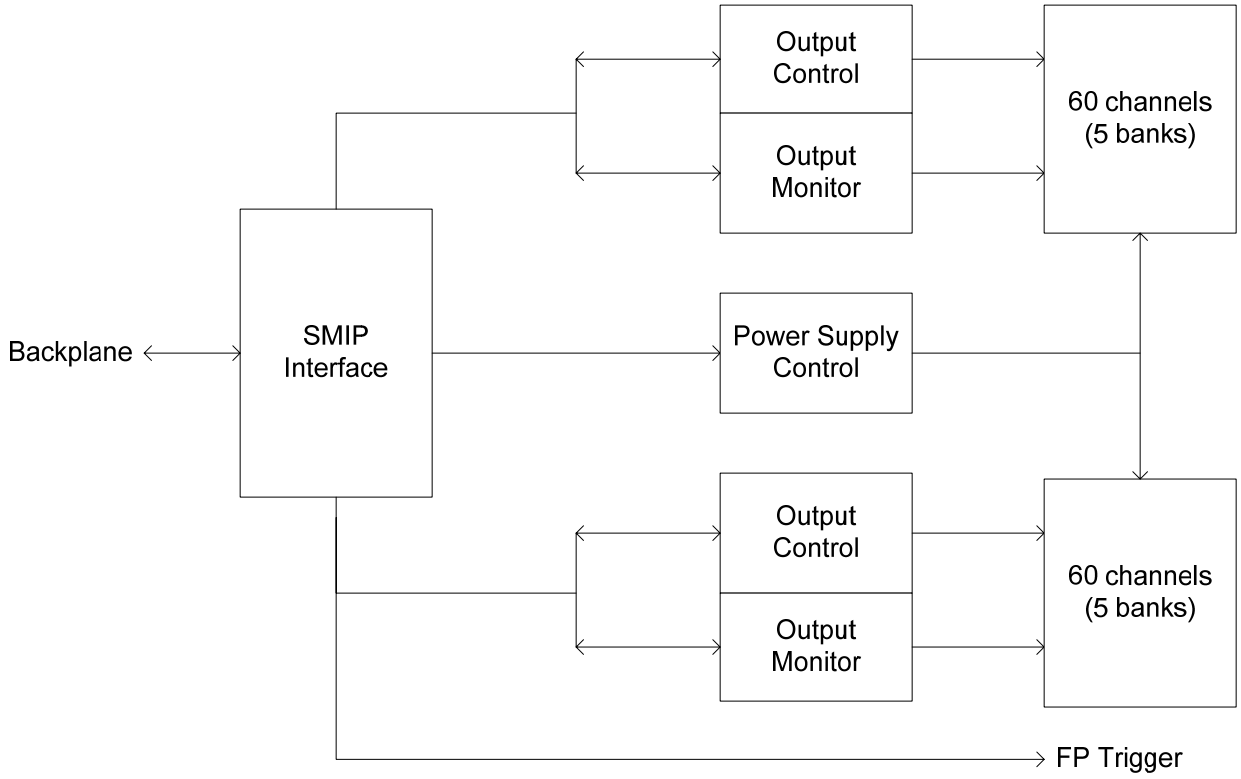

FIGURE 2-1: BASIC OPERATION DIAGRAM

Each section is further divided into five 12 channel banks (see Figure 2-2). Each bank of 12 channels is set to either 73 V (HI) and 2.5 V (LO) or 28 V (HI) and GND (LO). Each individual channel can be set to either HI, LO, or OFF. If a user, for example, sets bank 2 to 73 V, then channels 13 – 24 can be either 73 V, 2.5 V, or off. Similarly, if the user sets bank 6 to 28 V, then channels 61 – 72 can be either 28 V, GND, or off. Each channel is capable of sourcing/sinking up to 140 mA at 28 V. The maximum for the 73 V line is 1 mA. It is imperative to keep this in mind when operating the VT1802. Should an over-current condition (I > 140 mA) occur, the channel is shut off and an over-current event is registered for that channel. By accessing the ENABLE and LEVEL registers via the soft front panel, a channel can be set to ON/OFF or HI/LO, respectively. Each channel is additionally capable of Output Enable, Output Selection, and Output Level Readback.

NOTE	The 140 mA current capability should only be applied to the 28 V setting. If used in the 73 V setting, only ten channels can be used maximum. If more current is required, the power supply will lower to 28 V.

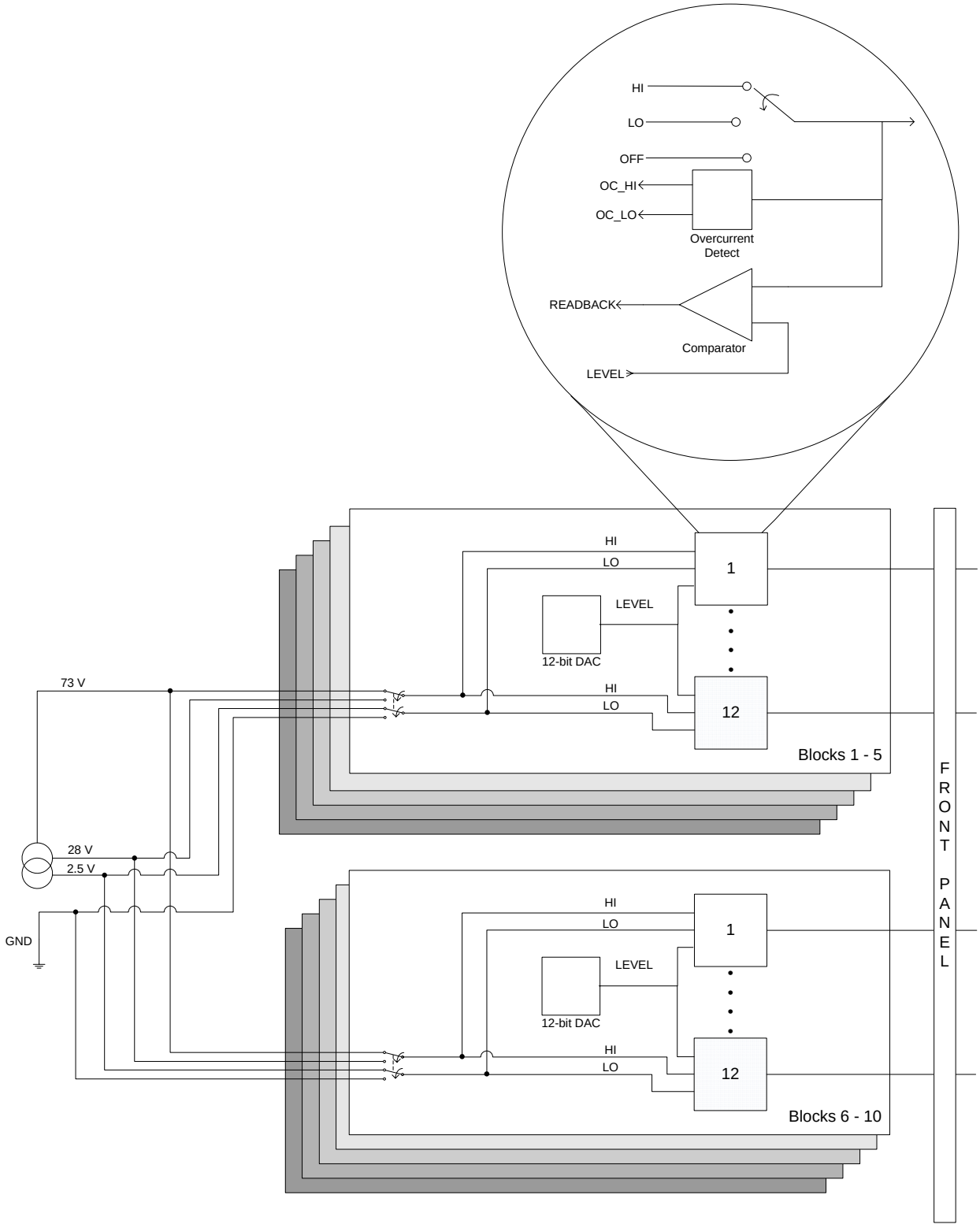

FIGURE 2-2: VT1802 BLOCK DIAGRAM

MODES OF OPERATION

Two different modes of operation are available on the VT1802. These modes are described below.

Mode	Explanation	Example
Single-ended	The channel can be configured to source current to or sink current from an external source	If a bank is set to 73 V/28 V, the channel will source up to 1 mA/140 mA (controlled by load). If a bank is set to 2.5 V/GND, the channel will sink up to 1 mA/140 mA (controlled by load)
Differential	Two channels of the same voltage are used, but set to different levels (73 V to 2.5 V or 28 V to GND) where one is used as the current source and one is used as a current sink.	If bank 2 is set to 28 V and GND, then channel 13 can be 28 V and connected to channel 24 (set at GND) via a proper load, or Bank 7 can be set to 73 V and 2.5 V, then channel 73 can be 73 V and connected to channel 84 (set at 2.5 V) via a proper load, or All channels from bank *x* set at either 28 V/73 V and connected to all channels from bank Y set at either GND/2.5 V. It is recommended that the latter example be used in practice for ease of use and to reduce the likelihood of making an incorrect wiring connection.
Note: the user must provide the appropriate load to avoid over-current.		

TRIGGER OPERATION

The VT1802 can be controlled via software. The user can issue commands to execute several functions: select channel, level, Select Bank Voltage, Over-current Status, etc. Two operations, Channel Output Enable and Channel Output Level Select, are used to engage the VT1802 when entered or via triggers supplied by any of the three following sources:

1) **External Trigger**: the VT1802 has two front panel connectors. They allow for 5 V TTL-level triggering and OR or AND operation can be selected.
2) **Backplane TTL0-7 Trigger**: There are eight backplane TTL trigger signals. These triggers are edge triggering and can be selected falling or rising edge triggering.
3) **Software Trigger**.

WARNINGS

1) If the external trigger experiences a voltage between 0.4 V and 2.4 V, the VT1802 may enter an indeterminate state. Measures should be taken to ensure that these conditions do not occur.
2) The external triggers are active-high level triggers that should be driven by a 5 V TTL signal. The signal must be free of glitches and stay in the high or low state for a minimum of 200 ns.
3) If the VT1802 external trigger experiences a voltage of greater than 6 V, damage will occur to the VT1802.

The priority of triggering is as following: EXT TRIGGERS, BACKPLANE TTL0-7 Trigger, Software Trigger. If all or many triggers are enabled, the highest priority will take precedent. The rest will be ignored.

In a trigger mode, the user first must set up the desired triggers by accessing the Command Trigger Control Register (see page 30). When the VT1802 is already in the trigger mode, any change to the Channel Output Enable and Channel Output Level Select will not be executed until:

1) Both EXT TRIG1 and EXT TRIG2 go to a TTL-high level (for AND setting), or
2) Either EXT TRIG1 or EXT TRIG2 goes to a TTL-high level (for OR setting), or
3) Any falling/rising edge on Backplane TTL0-7 Triggers line (for TTL Trigger setting and External Trigger is not enabled), or
4) Software trigger bit in the Trigger Control Register is set.

All other functions are not affected by triggering.

Channel output can be monitored via a comparator and a read-back register. The level of the comparator is set in a DAC in each bank. The DAC setting must take hysteresis and component variation into account.

CALCULATING HYSTERESIS

The following equation is used to calculate hysteresis for the VT1802:

$$= \quad Vut = (20/21)\,\mathrm{V} \times Vdac + (75/21)\,\mathrm{V}$$
$$Vlt = (20/21)\,\mathrm{V} \times Vdac$$

where:

Vut = upper threshold limit
Vlt = lower threshold limit
Vdac is the output of the DAC set by the user (LEVEL)
Vdac range = 0 V – 75 V
Vdac resolution = 75/4095 = 18.3 mV

Component variation error is ±3% for *Vdac*, hence, *Vut* and *Vlt* have a ±3% error as well.
The hysteresis voltage is 3.6 V for the whole range

Please note that, due to hysteresis, as *Vdac* is set to 0, the upper limit threshold, *Vut*, will be 3.6 V

MODULE INSTALLATION

Before installing a VT1802 module, make sure that the mainframe is powered down. Insert the module into the chassis by orienting the module so that the card guides of the module can be inserted into the slot of the chassis. Position the module so that it fits into the chassis slot groove. Once the module is properly aligned, push the module back and firmly insert it into the backplane connector.

FRONT PANEL CONNECTOR LOCATION ASSIGNMENTS

The Figure 2-3 illustrates the physical location assignments for each connector on the front panel of the module. This view depicts all connectors for both the VT1802.

The module's front panel LEDs may be monitored for an indication the VXI module's operation. The function of the LEDs is as follows:

LED Name	Function
Power	Illuminates green when power is applied to the module. Not illuminated when there is no power to the chassis. This LED is not programmable.
Error	Not illuminated under normal operating conditions. Illuminates red if an Error condition occurs. This LED is programmable.
Fail	Illuminates green under normal operating conditions. Illuminates red if an ac fail condition occurs. This LED is programmable.
Access	This LED flashes green when data is accesses or written to the VT1802's registers.

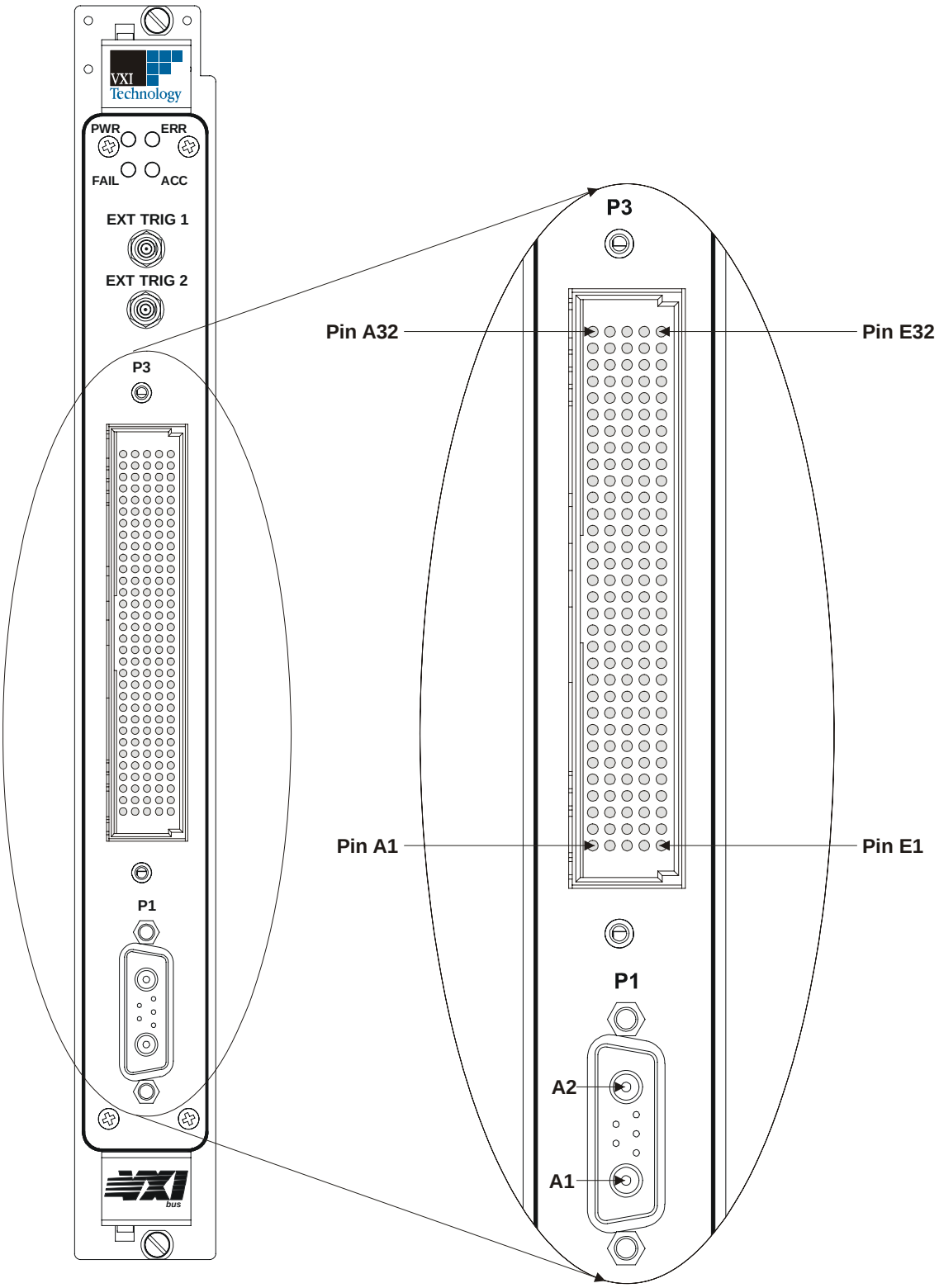

FIGURE 2-3: CONNECTOR LOCATION ASSIGNMENTS

TABLE 2-1: FRONT PANEL SIGNAL ASSIGNMENTS

ROW A	SIGNAL	ROW B	SIGNAL	ROW C	SIGNAL	ROW D	SIGNAL	ROW E	SIGNAL
1	CHN116	1	CHN117	1	CHN118	1	CHN119	1	CHN120
2	CHN111	2	CHN112	2	CHN113	2	CHN114	2	CHN115
3	CHN106	3	CHN107	3	CHN108	3	CHN109	3	CHN110
4	GND	4	GND	4	GND	4	GND	4	GND
5	CHN101	5	CHN102	5	CHN103	5	CHN104	5	CHN105
6	CHN96	6	CHN97	6	CHN98	6	CHN99	6	CHN100
7	CHN91	7	CHN92	7	CHN93	7	CHN94	7	CHN95
8	GND	8	GND	8	GND	8	GND	8	GND
9	CHN56	9	CHN57	9	CHN58	9	CHN59	9	CHN60
10	CHN51	10	CHN52	10	CHN53	10	CHN54	10	CHN55
11	CHN46	11	CHN47	11	CHN48	11	CHN49	11	CHN50
12	GND	12	GND	12	GND	12	GND	12	GND
13	CHN41	13	CHN42	13	CHN43	13	CHN44	13	CHN45
14	CHN36	14	CHN37	14	CHN38	14	CHN39	14	CHN40
15	CHN31	15	CHN32	15	CHN33	15	CHN34	15	CHN35
16	GND	16	GND	16	GND	16	GND	16	GND
17	GND	17	GND	17	GND	17	GND	17	GND
18	CHN26	18	CHN27	18	CHN28	18	CHN29	18	CHN30
19	CHN21	19	CHN22	19	CHN23	19	CHN24	19	CHN25
20	CHN16	20	CHN17	20	CHN18	20	CHN19	20	CHN20
21	GND	21	GND	21	GND	21	GND	21	GND
22	CHN11	22	CHN12	22	CHN13	22	CHN14	22	CHN15
23	CHN6	23	CHN7	23	CHN8	23	CHN9	23	CHN10
24	CHN1	24	CHN2	24	CHN3	24	CHN4	24	CHN5
25	GND	25	GND	25	GND	25	GND	25	GND
26	CHN86	26	CHN87	26	CHN88	26	CHN89	26	CHN90
27	CHN81	27	CHN82	27	CHN83	27	CHN84	27	CHN85
28	CHN76	28	CHN77	28	CHN78	28	CHN79	28	CHN80
29	GND	29	GND	29	GND	29	GND	29	GND
30	CHN71	30	CHN72	30	CHN73	30	CHN74	30	CHN75
31	CHN66	31	CHN67	31	CHN68	31	CHN69	31	CHN70
32	CHN61	32	CHN62	32	CHN63	32	CHN64	32	CHN65

NOTE

1) The 48 V input connector P1 is a 15-pin D-sub connector.
2) P1 is a D-sub connector with two pins, A1 and A2 for connection to power. A1 is +48 V and A2 is -48 V. **IT IS IMPERATIVE THAT THE POLARITY OF THESE CONNECTORS NOT BE REVERSED AS IT WILL CAUSE DAMAGE TO INTERNAL CIRCUITRY.** A mating connector and pins are provided with the unit.

SECTION 4

PROGRAMMING

INTRODUCTION

VT1802 modules are VXIbus register-based devices for high-speed data retrieval. Register-based programming is a series of **reads** and **writes** directly to the module's registers (this includes accesses to the modules RAM). This eliminates the time for command parsing thus increasing speed.

ADDRESSING

The VXI Technology switching modules utilize either the A24 or A32 space (set via the DIP switches on the bottom of the VT1802 module, see page 16) of the shared-memory architecture. To read or write to a module register, a register address needs to be specified. This is done by using the offset value (assigned by the resource manager) and multiplying it by 256 or 64 k to get the base address in A24 or A32 address space, respectively.

A24 Base Address = Offset value * 0x0100 *(or 256)*

A32 Base Address = Offset value * 0x10000 *(or 65,536)*

The A24 or A32 offset value, assigned by the resource manager, can also be accessed by reading the A16 Offset Register. To address the A16 Offset Register use the following formula:

A16 Base Address = (Logical Address * 64) + 0xC000 *(or 49,152)*

then

A16 Offset Register Address = A16 Base Address + 6

See A16 Memory Map on page 26 and the A24/A32 address space allocation on page 34.

TABLE 3-1: VT1802 REGISTER MAP - A16

OFFSET	WRITE FUNCTION	READ FUNCTION
0x3E	Trace Advance	Reserved
0x3C	Reserved	Reserved
0x3A	Trace RAM Control	Trace RAM Control
0x38	TTL Trigger Polarity	Reserved
0x36	Over-current Trigger Select & Power Enable	Reserved
0x34	Trace Advance Trigger Select	Reserved
0x32	Trace RAM Start Address LOW	Trace RAM Start Address LOW
0x30	Trace RAM Start Address HIGH	Trace RAM Start Address HIGH
0x2E	Trace RAM End LOW	Trace RAM End LOW
0x2C	Trace RAM End HIGH	Trace RAM End HIGH
0x2A	Trace RAM Restart LOW	Trace RAM Restart LOW
0x28	Trace RAM Restart HIGH	Trace RAM Restart HIGH
0x26	Command Trigger Control	Command Trigger Control
0x24	Output Control Function Bank Setup	Output Control Function Bank Setup
0x22	Output Control Function Bank Setup	Output Control Function Bank Setup
0x20	LED Control - NVM Access	LED Control - NVM Access
0x1E	Reserved	Subclass Register
0x1C	Interrupt Control	Interrupt Control
0x1A	Reserved	Interrupt Status
0x18	Reserved	Reserved
0x16	Reserved	Reserved
0x14	Reserved	Reserved
0x12	Reserved	Reserved
0x10	Reserved	Reserved
0x0E	Reserved	Version Number
0x0C	Reserved	Reserved
0x0A	Reserved	Reserved
0x08	Reserved	Reserved
0x06	Offset Register	Offset Register
0x04	Control Register	Status Register
0x00	Reserved	Device Type Register
0x00	LA Register	ID Register

NOTE If the VXI*plug&play* drivers are being used, these registers normally do not need to be accessed.

DESCRIPTION OF REGISTERS - A16

The following describes the registers shown in the VT1802 Register Map for A16 address space.

ID Register (0x00) — Read Only		
D11 - D0	Manufacturer's ID	VXI Technology, Inc., set to $F4B_{16}$
D13 - D12	Address Space	A16/A24 = 00_2 A16/A32 = 01_2
D15 - D14	Device Class	Extended register based device, set to 01_2

Logical Address Register (0x00) — Write Only		
D7 - D0	Logical Address	Sets the new logical address in a dynamically configured module. When set for dynamic configuration (set to FF_{16}) a soft reset will not alter the configured logical address, while a hard reset will set the register back to FF_{16}.
D15 - D8	Reserved	Writing to this range has no effect.

Device Type Register (0x02) — Read Only		
D11 - D0	Model Code	Model 296, set to 128_{16}
D15 - D12	Required Memory	2 MB, set to 2_{16}, for A24 2 MB, set to A_{16}, for A32

Status Register (0x04) — Read Only		
D15	A24/A32 Active	1 = Indicates that A24/A32 memory space access is enabled 0 = Indicates that A24/A32 memory space access is locked out
D14	MODID*	1 = Indicates that the module is not selected by the MODID line 0 = Indicates that the module is selected by the MODID line.
D13 - D4	Reserved	These bits always read as $11,1111,1111_2$
D3	Ready	This bit always reads as 1_2
D2	Passed	This bit always reads as 1_2
D1 - D0	Reserved	These bits always read as 11_2

Control Register (0x04) — Write Only		
D15	A24/A32 Enable	1 = Write a 1 to this bit to enable A24/A32 memory access 0 = To disable access
D14 – D2	Reserved	Writes to these bits have no effect.
D1	Sysfail Inhibit	Write a 1 to this bit to prevent the module from asserting the SYSFAIL* line.
D0	Reset	1 = Write a 1 to this bit to force the registers on the VT1802 interface into a reset state 0 = Write a 0 to release this soft reset state **Note: This does not reset output channels on the module.**

Offset Register (0x06) — Read & Write		
D15 - D0	A24/A32 Memory Offset	The value written to this 16-bit register multiplied by 256 sets the base address of the A24 memory space used by the module. The value written to this 16-bit register multiplied by 65,536 sets the base address of the A32 memory space used by the module. A read from this register reflects the previously written value. Because of the required memory size, bits D4-D0 are disregarded on writes and always read back as 0. Upon receiving a hard reset, all bits in this register are set to 0. A soft reset does not affect the value in this register.

Reserved Register (0x08) — Read Only		
D15 - D0	Unused	Always read back as $FFFF_{16}$

Reserved Register (0x0A) — Read Only		
D15 - D0	Unused	Always read back as $FFFF_{16}$

Reserved Register (0x0C) — Read Only		
D15 - D0	Unused	Always read back as $FFFF_{16}$

Version Number Register (0x0E) — Read Only		
D15 - D8	Firmware Version Number	Not applicable, reads back as 00_{16}
D7 - D0	Hardware Version Number	This code is incremented each time hardware changes are made to the VT1802 module VXI Interface FPGA.

Interrupt Status Register (0x1A) — Read Only		
D15	Scan Function done	The latest scan list update is complete.
D14 - D10	Unused	These bits are always read back as 0's.
D9	Over-current Error Detected Channels 61 thru 120	An Over-current event, either HI or LO, has occurred on a channel between 61 and 120. The OC registers for this bank must be queried to identify the channel(s) that indicated an Over-current Event. The Over-current event will reset the affected channel, effectively shutting it off. To turn the channel on again its Select bit must be re-set. See the A24/A32 Channel Select Register definitions on page 34.
D8	Over-current Error Detected Channels 1 thru 60	An Over-current event, either HI or LO, has occurred on a channel between 1 and 60. The OC registers for this bank must be queried to identify the channel/s that indicated an Over-current Event. The Over-current event will reset the affected channel, effectively shutting it off. To turn the channel on again its Select bit must be re-set. See the A24/A32 Channel Select Register definitions on page 34.
D7 - D0	Reserved	Always reads back as $FFFF_{16}$
Note: This status register may be used in a polled fashion rather than allowing the events above to generate an Interrupt. A read of this register will clear any active bits. Bits that are not set or are about to be set are not affected by a read of this register.		

Interrupt Control Register (0x1C) — Read & Write		
D15	Scan Function done mask bit	0 = Enabled 1 = Disabled
D14 – D10	Reserved	Writes to these bits have no effect.
D9	Over-current Error Event Channels 61 through 120	0 = Enabled 1 = Disabled
D8	Over-current Error Event Channels 1 thru 60	0 = Enabled 1 = Disabled
D7	IR ENA*	0 = Writing a 0 to this bit enables interrupter capabilities 1 = Writing a 1 to this bit disables interrupter capabilities
D6	IH ENA*	The module has no interrupt handler capability; therefore writing a 1 or 0 has no effect. A 1 is always read back for this bit.
D5 - D3	Interrupter IRQ Line	The complement of the value programmed into these three bits reflects the selected IRQ line used by the module. A value of 011_2 would select IRQ4, a value of 000_2 would select IRQ7, and a value of 111_2 would disconnect the IRQ lines.
D2 - D0	Handler IRQ Line	The module has no interrupt handler capability; therefore writing to these bits has no effect. A 111_2 is always read back for these bits.
Note that all bits in this register are set to 1 upon receipt of a hard or soft reset.		

Subclass Register (0x1E) — Read Only		
D15	VXIbus Extended Device	Always reads as 1.
D14 - D0	Extended Memory Device	Always reads as $7FFD_{16}$.

LED Control - NVM Access Register (0x20) — Read Only		
D15 – D9	Unused	All bits are always 1.
D8	Error LED Control	Reads back the value of ERROR LED.
D7 - D1	Unused	All bits are always 1.
D0		Reads back the serial data stream from the on board EEPROM device.

LED Control - NVM Access Register (0x20) — Write Only		
D15 – D9	Unused	Data written to these bits have no effect.
D8	Error LED Control	1 = Write a 1 to this bit to enable the front panel ERROR LED 0 = Write a 0 to this bit to disable the front panel ERROR LED
D7-D2	Unused	Data written to these bits have no effect.
D1		Serial clock for module; should be a logic 1 when not used.
D0		Serial data input; must be a logic 1 when not used.

Output Control Function Bank Setup Register (0x22, 0x24) — Read & Write		
D15 - D8		Always write 0x00.
D7 - D0		Register 0x22 sets the banks starting from Bank1 to Bank5 for Channel Output Control Function on Motherboard. Register 0x24 sets the banks starting from Bank6 to Bank10 for Channel Output Control Function on Daughterboard. Used in Trace Mode ONLY.

Command Trigger Control Register (0x26) — Read & Write		
D15	External Trigger 1 Enable	1 = Write a 1 to this bit to enable External Trigger 1 to control the transfer of data from the input buffer to the output buffer. 0 = Write a 0 to disable this trigger P_{on} state = 0
D14	External Trigger 2 Enable	1 = Write a 1 to this bit to enable External Trigger 2 to control the transfer of data from the input buffer to the output buffer. 0 = Write a 0 to disable this trigger P_{on} state = 0
D13	Backplane TTL0-7 Trigger	1 = Write a 1 to this bit to enable the VT1802 to execute user command if any bit TTLTRIG0-7 change edge as defined below. 0 = Write a 0 to disable this trigger P_{on} state = 0
D12	Software Trigger Enable	1 = Write a 1 to this bit to enable the VT1802 to execute user command if Software Trigger (bit D9) is set 0 = Write a 0 to disable this trigger P_{on} state = 1
D11	External Trig Control	1 = Write a 1 to this bit set the external triggers to: EXT TRIG1 AND EXT TRIG2 0 = Write a 0 to this bit set the external triggers to: EXT TRIG1 OR EXT TRIG2 P_{on} state = 0 For this bit's operation to be properly executed, both EXT TRIG1 and EXT TRIG2 must be enabled. When only one is enabled, this bit will be ignored.
D10	TTL Trig Polarity	0 sets the falling edge active 1 sets the rising edge active. P_{on} state = 0
D9	Software Trigger	1 = Write a 1 to trigger command execution 0 = Write a 0 to halt command execution P_{on} state = 0
D8	Unused	Data written to this bit have no effect and always read back as 1.
D7-0	Software Trigger	Sets the TTLTRIG line or lines, which are configured as inputs, and will trigger the VT1802 to execute command from user. D7 corresponds to TTLTRIG7, D6 to TTLTRIG6, … and D0 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All enabled TTLTRIG lines are OR'd together to allow more than one TTLTRIG line to cause a Command Execution Trigger event to occur. All bits are set to 0 when the module receives either a soft or a hard reset. **Note: This is different from the setup of register 0x34.**

NOTE	The priority of triggering is as following: EXT TRIG1, EXT TRIG2, TTLTRIG0-7, and SOFTWARE. If all or many triggers are enabled, the highest priority will take precedent. The rest will be ignored. TTLTRIG0-7 will be edge triggering only. The trigger will only affects the following A24/A32 output commands: Channel Output Enable, and Channel Output Level Select. All other A24/A32 commands and A16 will not be affected.

Trace RAM Restart High Register (0x28) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets the four most significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM Restart Low Register (0x2A) — Read & Write		
D15 - D0		Sets the 16 least significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM End High Register (0x2C) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets the four most significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM End Low Register (0x2E) — Read & Write		
D15 - D0		Sets the 16 least significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM Start Address HIGH Register (0x30) — Read & Write		
D15 - D4	Unused	Data written to these bits have no effect and always read back as 1.
D3 - D0		Sets and reads back the four most significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed.

Trace RAM Start Address LOW Register (0x32) — Read & Write		
D15 - D0		Sets and reads back the sixteen least significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed.

Trace Advance Trigger Select Register (0x34) — Write Only		
D15 - D8		Sets the TTLTRIG line or lines, which are configured as outputs, and will toggle when Trace Advance condition occurs in the module. D15 corresponds to TTLTRIG7, D14 to TTLTRIG6, … and D8 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All bits are set to 0 when either a soft or a hard reset is received by the module.
D7 - D0		Sets the TTLTRIG line or lines, which are configured as inputs, and will cause a Trace Advance event to occur in the module. D7 corresponds to TTLTRIG7, D6 to TTLTRIG6, … and D0 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All enabled TTLTRIG lines are OR'd together to allow more than one TTLTRIG line to cause a Trace Advance event to occur. All bits are set to 0 when the module receives either a soft or a hard reset.

Over-current Trigger Select & Power Enable Register (0x36) — Read-Write		
D15 - D8		Sets the TTLTRIG line or lines, which are configured as outputs, and will toggle when either bank 1 to 60 or 61 to 120 Over-current Event conditions occur in the module. D15 corresponds to TTLTRIG7, D14 to TTLTRIG6, … and D8 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All bits are set to 0 when either a soft or a hard reset is received by the module.
D7 – D4	Unused	Data written to these bit have no effect
D3	73 V Power Supply Status	1 = The 73 V on-board power supply is ON 0 = The 73 V on-board power supply is OFF
D2	28 V Power Supply Status	1 = The 28 V on-board power supply is ON 0 = The 28 V on-board power supply is OFF
D1	73 V Power Supply Enable	1 = Write a 1 to this bit to enable the 73 V on-board power supply 0 = Write a 0 to this bit to disable the 73 V on-board power supply P_{on} state = 0 **Note: This bit must be set in order for the module's outputs to function properly.**
D0	28 V Power Supply Enable	1 = Write a 1 to this bit to enable the 28 V on-board power supply 0 = Write a 0 to this bit to disable the 28 V on-board power supply P_{on} state = 0 **Note: This bit must be set in order for the module's outputs to function properly.**

TTL Trigger Polarity Register (0x38) — Write Only		
D15 – D3	Unused	Data written to these bits have no effect.
D2	Over-current Event Output Slope	0 sets the falling edge active, 1 sets the rising edge active.
D1	Trace Advance Input Slope	0 advances on the falling edge, 1 advances on the rising edge.
D0	Trace Advance Output Slope	0 sets the falling edge active, 1 sets the rising edge active.
Note: A hard or a soft reset sets D3 - D0 to 0 s.		

Trace RAM Control Register (0x3A) — Read & Write		
D15 - D14	Unused	Must be set to 11. Set to 11 at power on.
D13 - D10	Function Enabled	D13 is for Channel Output Monitor Function – Section 2 (Daughterboard) D12 is for Channel Output Control Function – Section 2 (Daughterboard) D11 is for Channel Output Monitor Function – Section 1 (Motherboard) D10 is for Channel Output Control Function – Section 1 (Motherboard) Set to 0 to enabled the function. Set to a 1 if not used. These bits are set to 0000 at power on.
D9-D8	Unused	Must be set to 00
D7 - D4	Function used in trace mode	D7 is for Channel Output Monitor Function – Section 2 (Daughterboard) D6 is for Channel Output Control Function – Section 2 (Daughterboard) D5 is for Channel Output Monitor Function – Section 1 (Motherboard) D4 is for Channel Output Control Function – Section 1 (Motherboard) Set to 1 if Function is used in trace mode, set to 0 if not in trace mode. At power on all bits are set to 0. For standard VT1802 trace mode, only D6 and D4 are set active. Note: D7 and D4 are for Channel Output Monitor Controls, which should not be used in trace mode. Setting D7 and D4 bits to 1 could produce very unexpected results while running in trace mode.
D3 - D2	Unused	Data written to these bits have no effect. The value written is read back.
D1	LOOP ENABLE	1 = enabled 0 = disabled. If enabled, the trace resumes at the start of active RAM and continues from there. If disabled, the trace stops at the end of active RAM and clears the TRACE ENABLE bit.
D0	TRACE ENABLE	1 = enabled 0 = disabled. If the LOOP ENABLE bit is set and the end of active trace RAM is reached, this bit will not be reset.

Reserved Registers (0x3C) — Read & Write		
D15 – D0	Unused	Writing to these registers has no effect. Read back value is register dependent.

Trigger Advance Register (0x3E) — Write Only		
D15 - D0	Unused	The act of writing to this location causes a Trace Advance event to occur in the module. The specific data written to these bits has no effect.

DESCRIPTION OF VT1802 MODULE REGISTERS - A24 / A32 - EXTENDED MEMORY

The VT1802 contains 2 identical sections, 60 channels per section. Each section is assigned 2 kB (2048 bytes) of memory as shown in the VT1802 Configuration/Register Map for A24/A32 address space. The following describes these registers.

Section 1 - Channel Output Enable Register — Read & Write		
ADDR	A24/A32 Offset +0x000/0x004/0x008/0x00C/0x010	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Channel 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1 Select	**Channel Select bits**: By setting these bits, the associated channel is turned on (enabled). These bits are cleared by an over-current event on a per channel basis. The corresponding bits in the Over-current registers can be used to identify channels that have experienced an over-current event. See *Over-current Register* definition below. Once a channel has experienced an over-current event, the Channel Select bit must again be set to a "1" to allow the channel to source its programmed output voltage. 0 = Channel disabled 1 = Channel enabled P_{on} state = 0 **NOTE: If a Channel fails to operate properly or as expected, then a read of the channel's Over-current bit may be required to determine whether the channel has experienced an over-current event or not.**

Section 1 - Channel Output Level Select Register — Read & Write		
ADDR	A24/A32 Offset +0x002/0x006/0x00A/0x00E/0x012	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Channels 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1	**Channel bits**: By setting these bits, the associated channel is set HI or LO. These bits are not affected by an over-current event. The actual V_{out} HI and V_{out} LO of the channel is set by the *Voltage Level Control* for the associated channel. See page 36 for more information on the *Voltage Level Control* register. 0 = Channel output LO 1 = Channel output HI P_{on} state = 0

Section 1 - Channel Over-current Status LO Register — Read Only		
ADDR	A24/A32 Offset +0x014/0x018/0x01C/0x020/0x024	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1	**Channel Over-current LO Status bits:** A "1" indicates that a V_{out} LO Over-current Event has occurred. A "0" indicates no Over-current Event has occurred. An over-current event will set the appropriate Over-current Status bit and will also *disable the associated channel's Channel Select bit*. Once disabled, the channel may again be enabled by setting the channel's Channel Select bit to "1". See the *Channel Select Register* description above. The bits contained in these registers provide status only and do not affect the operation of the associated channels. A read of these registers will clear the Over-current Status bits in the associated register to "0". Removing the over-current condition does not reset these bits. Once set, the bits are not cleared except until there is a read of the associated register. A recurrent over-current event will again disable the associated channel by resetting the channel's Channel Select bit. It will also set the *Channel Over-current Status* bit. If the status bit had not been cleared, it will remain a "1".

Section 1 - Channel Over-current Status HI Register — Read Only		
ADDR	A24/A32 Offset +0x016/0x01A/0x01E/0x022/0x026	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1	**Channel Over-current HI Status bits**: A "1" indicates that a V_{out} HI Over-current Event has occurred. A "0" indicates no over-current event has occurred. An over-current event will set the appropriate Over-current Status bit and will also *disable the associated channel's Channel Select bit*. Once disabled, the channel may again be enabled by setting the channel's Channel Select bit to "1". See the *Channel Select register* description above. The bits contained in these registers provide status only and do not affect the operation of the associated channels. A read of these registers will clear the Over-current Status bits in the associated register to "0". Removing the over-current condition does not reset these bits. Once set, the bits are not cleared except until there is a read of the associated register. A recurrent over-current event will again disable the associated channel by resetting the channel's Channel Select bit. It will also set the *Channel Over-current Status* bit. If the status bit had not been cleared, it will remain a "1".

Section 1 - Voltage Level Control Register — Read & Write		
ADDR	A24/A32 Offset + 0x200	
D15 – D13	Unused	Writing to these bits has no effect. Read back value is what was written.
D12	Channel 60 – 49 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D11	Channel 48 – 37 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D10	Channel 36 – 25 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D9	Channel 24 – 13 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D8	Channel 12 – 1 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D7 – D5	Unused	Writing to these registers has no effect. Read back value is what is written.
D4	Channel 60 – 49 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D3	Channel 48 – 37 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D2	Channel 36 – 25 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D1	Channel 24 – 13 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D0	Channel 12 – 1 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0

Section 1 - Channel Output Hardware Revision Register — Read Only		
ADDR	A24/A32 Offset +0x202	
D15 – D8	Unused	Always reads as 00_{16}
D7 - D0	Hardware Revision Code	This code is incremented each time hardware changes are made to the VT1802 module Channel Output FPGA.

Section 1 - Channel Monitor Output Status Register — Read Only		
ADDR	A24/A32 Offset +0x428/0x42A/0x42C/0x42E/0x430	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1	Channel Output Status bits: A "1" indicates that the channel is currently outputting, or is experiencing, a V_{out} HI condition. A "0" indicates that the channel is currently outputting, or is experiencing, a V_{out} LO condition. To create the Channel Output Status bits, the channel's output voltage is compared to a threshold reference voltage that is set in the *Channel Output Threshold Voltage* register. See the *Channel Output Threshold Voltage* register description below. These bits may be used to monitor for the proper operation of the module's output channels. NOTE: Each channel's output status comparator has about 4.0 V of hysteresis.

Section 1 - Channel Monitor Output Threshold Voltage Register— Read & Write		
ADDR	A24/A32 Offset +0x604/0x606/0x608/0x60A/0x60C	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Reference Voltage for Channels 60 - 49 48 - 37 36 - 25 24 - 13 12 – 1	Channel Output Threshold Voltage bits: The value written to these bits set the threshold voltage that will be used to indicate the channel's Output Status. If the channel's output voltage is *above* the threshold set, then the channel's Output Status bit will indicate a "1". If the channel's output voltage is *below* the threshold set, then the channel's Output Status bit will indicate a "0". See the *Channel Output Status Register* description above. The actual V_{out} HI and V_{out} LO of the channel is set by the *Voltage Level Control* bits for the associated channel. See the *Voltage Level Control* register above. 0x000 = Channel Output Threshold set to 0 V (minimum) 0xFFF = Channel Output Threshold set to approx. 75 V (maximum) P_{on} state = 0x000 Example: Set register 0x208 to a value of 0x802. The threshold voltage for channels 36 thru 25 is set to 0x802/0xFFF * 75 = 2050/4095 * 75 = 0.500 * 75 ≈ 37.5 volts. Note: Each channel's output status comparator has about 4.0 V of hysteresis.

Section 1 - Channel Monitor Hardware Revision Register — Read Only		
ADDR	A24/A32 Offset +0x60E	
D15 – D8	Unused	Always reads as 00_{16}
D7 - D0	Hardware Revision Code	This code is incremented each time hardware changes are made to the VT1802 module Channel Monitor FPGA.

Section 2 - Channel Output Enable Register — Read & Write		
ADDR	A24/A32 Offset +0x800/0x804/0x808/0x80C/0x810	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Channel 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61 Select	Channel Select bits: By setting these bits, the associated channel is turned on (enabled). These bits are cleared by an over-current event on a per channel basis. The corresponding bits in the Over-current registers can be used to identify channels that have experienced an over-current event. See *Over-current Register* definition below. Once a channel has experienced an over-current event, the Channel Select bit must again be set to a "1" to allow the channel to source its programmed output voltage. 0 = Channel disabled 1 = Channel enabled P_{on} state = 0 NOTE: If a Channel fails to operate properly or as expected, then a read of the channel's Over-current bit may be required to determine whether the channel has experienced an over-current event or not.

Section 2 - Channel Output Level Select Register — Read & Write		
ADDR	A24/A32 Offset +0x802/0x806/0x80A/0x80E/0x812	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Channels 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61	Channel bits: By setting these bits, the associated channel is set HI or LO. These bits are not affected by an over-current event. The actual V_{out} HI and V_{out} LO of the channel is set by the *Voltage Level Control* for the associated channel. See page 40 for more information on the *Voltage Level Control* register. 0 = Channel output LO 1 = Channel output HI P_{on} state = 0

Section 2 - Channel Over-current Status LO Register — Read Only		
ADDR	A24/A32 Offset +0x814/0x818/0x81C/0x820/0x824	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61	Channel Over-current LO Status bits: A "1" indicates that a V_{out} LO Over-current Event has occurred. A "0" indicates no Over-current Event has occurred. An over-current event will set the appropriate Over-current Status bit and will also *disable the associated channel's Channel Select bit*. Once disabled, the channel may again be enabled by setting the channel's Channel Select bit to "1". See the *Channel Select Register* description above. The bits contained in these registers provide status only and do not affect the operation of the associated channels. A read of these registers will clear the Over-current Status bits in the associated register to "0". Removing the over-current condition does not reset these bits. Once set, the bits are not cleared except until there is a read of the associated register. A recurrent over-current event will again disable the associated channel by resetting the channel's Channel Select bit. It will also set the *Channel Over-current Status* bit. If the status bit had not been cleared, it will remain a "1".

Section 2 - Channel Over-current Status HI Register — Read Only		
ADDR	A24/A32 Offset +0x816/0x81A/0x81E/0x822/0x826	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61	Channel Over-current HI Status bits: A "1" indicates that a V_{out} HI Over-current Event has occurred. A "0" indicates no over-current event has occurred. An over-current event will set the appropriate Over-current Status bit and will also *disable the associated channel's Channel Select bit*. Once disabled, the channel may again be enabled by setting the channel's Channel Select bit to "1". See the *Channel Select Register* description above. The bits contained in these registers provide status only and do not affect the operation of the associated channels. A read of these registers will clear the Over-current Status bits in the associated register to "0". Removing the over-current condition does not reset these bits. Once set, the bits are not cleared except until there is a read of the associated register. A recurrent over-current event will again disable the associated channel by resetting the channel's Channel Select bit. It will also set the *Channel Over-current Status* bit. If the status bit had not been cleared, it will remain a "1".

Section 2 - Voltage Level Control Register — Read & Write		
ADDR	A24/A32 Offset + 0xA00	
D15 – D13	Unused	Writing to these bits has no effect. Read back value is what was written.
D12	Channel 120 – 109 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D11	Channel 108 – 97 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D10	Channel 96 – 85 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D9	Channel 84 – 63 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D8	Channel 72 – 61 V_{out} HI	0 = V_{out} HI is +28 V 1 = V_{out} HI is +73 V P_{on} state = 0
D7 – D5	Unused	Writing to these registers has no effect. Read back value is what is written.
D4	Channel 120 – 109 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D3	Channel 108 – 97 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D2	Channel 96 – 85 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D1	Channel V_{out} – 63 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0
D0	Channel 72 – 61 V_{out} LO	0 = V_{out} LO is ground 1 = V_{out} LO is +2.5 V P_{on} state = 0

Section 2 - Channel Output Hardware Revision Register — Read Only		
ADDR	A24/A32 Offset +0xA02	
D15 – D8	Unused	Always reads as 00_{16}
D7 - D0	Hardware Revision Code	This code is incremented each time hardware changes are made to the VT1802 module Channel Output FPGA.

Section 2 - Channel Monitor Output Status Register — Read Only		
ADDR	A24/A32 Offset +0xC28/0xC2A/0xC2C/0xC2E/0xC30	
D15 – D12	Unused	All bits are always 0.
D11 - D0	Channels 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61	Channel Output Status bits: A "1" indicates that the channel is currently outputting, or is experiencing, a V_{out} HI condition. A "0" indicates that the channel is currently outputting, or is experiencing, a V_{out} LO condition. To create the Channel Output Status bits, the channel's output voltage is compared to a threshold reference voltage that is set in the *Channel Output Threshold Voltage* register. See the *Channel Output Threshold Voltage* register description below. These bits may be used to monitor for the proper operation of the module's output channels. Note: Each channel's output status comparator has about 4.0 V of hysteresis.

Section 2 - Channel Monitor Output Threshold Voltage Register— Read & Write		
ADDR	A24/A32 Offset +0xE04/0xE06/0xE08/0xE0A/0xE0C	
D15 – D12	Unused	Writing to these bits has no effect. Read back value is what was written.
D11 - D0	Reference Voltage for Channels 120 - 109 108 - 97 96 - 85 84 - 73 72 – 61	Channel Output Threshold Voltage bits: The value written to these bits set the threshold voltage that will be used to indicate the channel's Output Status. If the channel's output voltage is *above* the threshold set, then the channel's Output Status bit will indicate a "1". If the channel's output voltage is *below* the threshold set, then the channel's Output Status bit will indicate a "0". See the *Channel Output Status Register* description above. The actual V_{out} HI and V_{out} LO of the channel is set by the *Voltage Level Control* bits for the associated channel. See the *Voltage Level Control* register above. 0x000 = Channel Output Threshold set to 0 V (minimum) 0xFFF = Channel Output Threshold set to approx. 75 V (maximum) P_{on} state = 0x000 Example: Set register 0x208 to a value of 0x802. The threshold voltage for channels 36 thru 25 is set to 0x802/0xFFF * 75 = 2050/4095 * 75 = 0.500 * 75 ≈ 37.5 V. Note: Each channel's output status comparator has about 4.0 V of hysteresis.

Section 2 - Channel Monitor Hardware Revision Register — Read Only		
ADDR	A24/A32 Offset +0xE0E	
D15 – D8	Unused	Always reads as 00_{16}
D7 - D0	Hardware Revision Code	This code is incremented each time hardware changes are made to the VT1802 module Channel Monitor FPGA.

USING THE CODE

Wrap Around Test Example

The following pages provide sample code for performing a wrap around self-test. A block diagram is also provided to show how the VT1802 should be configured and wired to perform this test.

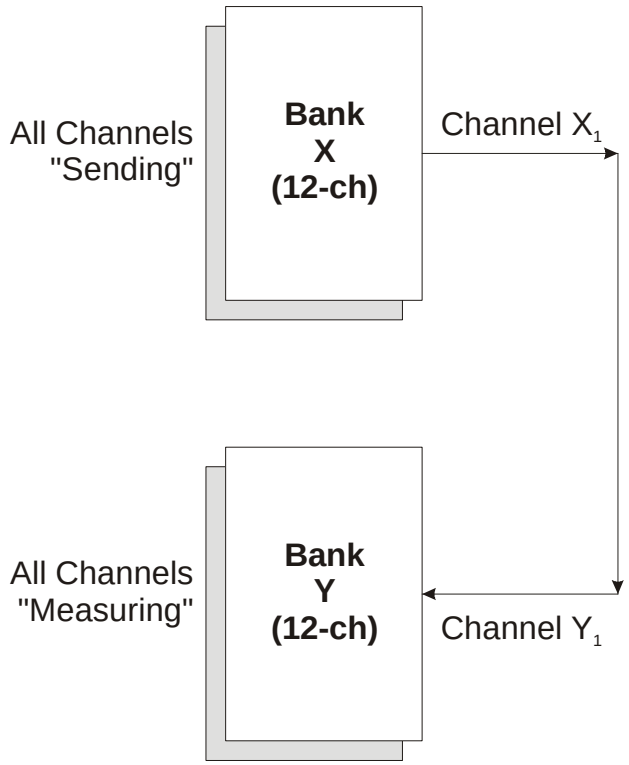

FIGURE 3-1: WRAP AROUND SELF-TEST DIAGRAM

Required Settings for "Measuring Bank":

- Channel Output = DISABLED
- Channel Output Level set, preferably, to LOW and Bank Voltage Level set to 0 V/28 V (i.e. 0 V) to avoid sourcing current if the Channel Output is mistakenly changed to ENABLE.
- On the "Measuring Bank," the DAC settings can be varied to measure the voltage from the "sending" channel. Hysteresis must be taken into account. Refer to page 21 for hysteresis calculations. Note, there is only 1 DAC per bank.

The "Sending Bank" settings can be set the same as for normal Output operation:

- Channel Output = ENABLED
- Bank Voltage Level = 0 V/28 V or 2.5 V/73 V
- Channel Level = HI or LOW

NOTE	All channels in the "measuring" bank must have their output disabled to ensure proper operation. It is imperative that all three conditions listed above for the "measuring channel be met. Failure to do so can result in damage to the VT1802.

The following pages provide code for the wrap around test.

```
// - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
//      wrapTest.c
// - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
//      wrapTest1802() output from bank 1, input from bank 2 - requires bank 1 to be wired to bank 2
// - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int CVICALLBACK wrapTest1802(int panel, int control, int event, void *cbD, int eD1, int eD2)
{       ViStatus        iStatus;
        ViInt16         tmpBank, regData, regSele, pwrCtrl;
        ViInt16         inpBank, outBank, inpData, outData;
        ViReal64        ctVolts, dlyTime;
        int             gStatus, i, j;

        switch (event)
        {       case EVENT_COMMIT:
                        pwrCtrl = vtvm1802_LOG1_PWR_28V;                                //      comment out the one you don't want
//                      pwrCtrl = vtvm1802_LOG1_PWR_73V;
                        ctVolts = (pwrCtrl == vtvm1802_LOG1_PWR_73V) ? 36.5 : 14.0 ;

                        dlyTime = 0.1;

                        outBank = 1;                                                    //      our test board is bank 1 - bank 2
                        inpBank = 2;
                        regData = 0x0000;
                        regSele = vtvm1802_PIN_ENAB_REG;
                        for(i = 0; i < 5; i++)                                          //      disable all banks
                        {       tmpBank = outBank + i;                                  //      setup the pin bank
                                iStatus = vtvm1802_setBankData(instHndl, tmpBank, regSele, regData);
                                if(iStatus < VI_SUCCESS)
                                        MessagePopup("ERROR", "_setBankData() failed");
                        }
                        //      all banks disabled, turn on the power
                        iStatus = vtvm1802_setPowerCtrl(instHndl, pwrCtrl);             //      power on
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setPowerCtrl() failed");
                        iStatus = vtvm1802_setBankLevel(instHndl, inpBank, 0, pwrCtrl); //      set logic 1 level
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setBankLevel() failed, input bank logic 1 level");
                        iStatus = vtvm1802_setBankLevel(instHndl, outBank, 0, pwrCtrl); //      set logic 1 level
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setBankLevel() failed, output bank logic 1 level");

                        iStatus = vtvm1802_setCompLevel(instHndl, inpBank, ctVolts);    //      set comparator
                        if(iStatus < VI_SUCCESS)                                        //      threshold for the
                                MessagePopup("ERROR", "_setCompLevel() failed, input bank"); //  input and
                        iStatus = vtvm1802_setCompLevel(instHndl, outBank, ctVolts);    //      output banks
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setCompLevel() failed, output bank");

                        regSele = vtvm1802_PIN_HILO_REG;
                        for(i = 0; i < 5; i++)                                          //      make all outputs low
                        {       tmpBank = i + 1;                                        //      the pin bank numbers are 1 based
                                iStatus = vtvm1802_setBankData(instHndl, tmpBank, regSele, regData);
                                if(iStatus < VI_SUCCESS)
```

```
                MessagePopup("ERROR", "_setBankData() failed, clear Hi/Lo reg");
}
gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
Delay(dlyTime);

regData = 0x0FFF;                                       //      enable output bank
regSele = vtvm1802_PIN_ENAB_REG;                        //      select bank enable register
iStatus = vtvm1802_setBankData(instHndl, outBank, regSele, regData);
if(iStatus < VI_SUCCESS)
    MessagePopup("ERROR", "_setBankData() failed, enable output bank");
regData = 0x0000;                                       //      disable input bank
iStatus = vtvm1802_setBankData(instHndl, inpBank, regSele, regData);
if(iStatus < VI_SUCCESS)
    MessagePopup("ERROR", "_setBankData() failed, disable input bank");

outData = 0x0001;                                       //      we're going to walk a 1
for(j = 0; j < 12; j++)
{
    //      write the data to the Hi/Lo register
    iStatus = vtvm1802_setBankData(instHndl, outBank, vtvm1802_PIN_HILO_REG, outData);
    if(iStatus < VI_SUCCESS)
        MessagePopup("ERROR", "_setBankData() failed");
    gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
    Delay(dlyTime);
    //      check what we wrote to the Hi/Lo register
    iStatus = vtvm1802_getBankData(instHndl, outBank, vtvm1802_PIN_HILO_REG, &inpData);
    if(iStatus < VI_SUCCESS)
        MessagePopup("ERROR", "_getBankData() failed");
    if(inpData != outData)
        MessagePopup("ERROR", "Output bank read data not equal to write data");
    gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
    Delay(dlyTime);
    //      now read the data from the output bank readback register
    iStatus = vtvm1802_getBankData(instHndl, outBank, vtvm1802_PIN_RDBK_REG, &inpData);
    if(iStatus < VI_SUCCESS)
        MessagePopup("ERROR", "_getBankData() failed");
    if(inpData != outData)
        MessagePopup("ERROR", "Output bank readback data not equal to output bank write data");
    gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
    Delay(dlyTime);
    //      now read the data from the input bank readback register
    iStatus = vtvm1802_getBankData(instHndl, inpBank, vtvm1802_PIN_RDBK_REG, &inpData);
    if(iStatus < VI_SUCCESS)
        MessagePopup("ERROR", "_getBankData() failed");
    if(inpData != outData)
        MessagePopup("ERROR", "Input bank readback data not equal to output bank write data");

    gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
    Delay(dlyTime);

    outData <<= 1;
}
```

```
                outBank = 1;                                    //      our test board is bank 1 - bank 2
                inpBank = 2;
                regData = 0x0000;
                regSele = vtvm1802_PIN_ENAB_REG;
                for(i = 0; i < 5; i++)                          //      disable all banks
                {       tmpBank = outBank + i;                  //      setup the pin bank
                        iStatus = vtvm1802_setBankData(instHndl, tmpBank, vtvm1802_PIN_ENAB_REG, regData);
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setBankData() failed");
                        iStatus = vtvm1802_setBankData(instHndl, tmpBank, vtvm1802_PIN_HILO_REG, regData);
                        if(iStatus < VI_SUCCESS)
                                MessagePopup("ERROR", "_setBankData() failed");
                }

                gStatus = dpyUpd1802(mainHndl, MAIN_RDPY, EVENT_COMMIT, VI_NULL, 0, 0);
                Delay(dlyTime);

                break;
        }
        return(0);
}

// - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
//      dpyUpd1802()    refresh instrument display
// - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int CVICALLBACK dpyUpd1802(int panel, int control, int event, void *cbD, int eD1, int eD2)
{       ViStatus        iStatus = VI_SUCCESS;
        ViInt16         pinBank, pinChan, regMask, regSele;     //      pdState,
        ViInt16         enaData, regData, rbkData, ochData, oclData;
        int             pinEnab, regEnab, rbkEnab, ochEnab, oclEnab;
        int             gStatus, frsBank, i, j;                 //      lclCtrl,
        int             ledEnab, ledHiLo, ledRdbk, ledOchi, ledOclo;

        switch (event)
        {       case EVENT_COMMIT:
                        getFrsBnk(&frsBank);
                        regSele = vtvm1802_PIN_ENAB_REG;        //      display the enables
                        ledEnab = MAIN_B1PE_1;
                        ledHiLo = MAIN_B1PL_1;
                        ledRdbk = MAIN_B1RB_1;
                        ledOchi = MAIN_B1OH_1;
                        ledOclo = MAIN_B1OL_1;

                        for(i = 0; i < 5; i++)                  //      do 5 pin banks
                        {       pinBank = frsBank + i;          //      pin bank numbers are 1 based
                                //      read the registers
                                iStatus = vtvm1802_getBankData(instHndl, pinBank, vtvm1802_PIN_ENAB_REG, &enaData);
                                iStatus = vtvm1802_getBankData(instHndl, pinBank, vtvm1802_PIN_HILO_REG, &regData);
                                iStatus = vtvm1802_getBankData(instHndl, pinBank, vtvm1802_PIN_RDBK_REG, &rbkData);
                                iStatus = vtvm1802_getBankData(instHndl, pinBank, vtvm1802_PIN_OCHI_REG, &ochData);
                                iStatus = vtvm1802_getBankData(instHndl, pinBank, vtvm1802_PIN_OCLO_REG, &oclData);

                                regMask = 1;
```

```
                    for(j = 0; j < 12; j++)
                    {       pinChan = j + 1;
                            pinEnab = ((enaData & regMask) == regMask) ? 1 : 0;
                            regEnab = ((regData & regMask) == regMask) ? 1 : 0;
                            rbkEnab = ((rbkData & regMask) == regMask) ? 1 : 0;
                            ochEnab = ((ochData & regMask) == regMask) ? 1 : 0;
                            oclEnab = ((oclData & regMask) == regMask) ? 1 : 0;
                            gStatus = SetCtrlVal(mainHndl, ledEnab, pinEnab);
                            gStatus = SetCtrlVal(mainHndl, ledHiLo, regEnab);
                            gStatus = SetCtrlVal(mainHndl, ledRdbk, rbkEnab);
                            gStatus = SetCtrlVal(mainHndl, ledOchi, ochEnab);
                            gStatus = SetCtrlVal(mainHndl, ledOclo, oclEnab);
                            if(pinEnab)
                            {       gStatus = SetCtrlAttribute(mainHndl, ledHiLo, ATTR_OFF_COLOR, VAL_BLUE);
                                    gStatus = SetCtrlAttribute(mainHndl, ledHiLo, ATTR_ON_COLOR, VAL_RED);
                            }
                            else
                            {       gStatus = SetCtrlAttribute(mainHndl, ledHiLo, ATTR_OFF_COLOR, VAL_LT_GRAY);
                                    if(ochEnab || oclEnab)                  //      if overload, it's open regardless of cmd
state
                                            gStatus = SetCtrlAttribute(mainHndl, ledHiLo, ATTR_ON_COLOR, VAL_LT_GRAY);
                                    else
                                            gStatus = SetCtrlAttribute(mainHndl, ledHiLo, ATTR_ON_COLOR, VAL_GREEN);
                            }

                            ledEnab += 1;                                   //      next enab led control
                            ledHiLo += 1;                                   //      next hilo
                            ledRdbk += 1;                                   //      next rdbk
                            ledOchi += 1;                                   //      next ochi
                            ledOclo += 1;                                   //      next oclo

                            regMask <<= 1;                                  //      shift the register mask
                    }
            }
            DisplayPanel(mainHndl);
            break;
    }
    return 0;
}
```

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